Knowledge-based design of low-power analog integrated circuits

Mehdi Dolatshahi 1, Mostafa Alimosaymer 2, Omid Hashemipour 3, Maziar Mehrabi 4

1 Department of Electrical Engineering, Science and Research Branch, Islamic Azad University, Tehran, IRAN
2 Young researchers club, Islamic Azad University, Najafabad Branch, IRAN
3 Department of Electrical Engineering, Shahid Beheshti University, G. C, Tehran, IRAN
4 Department of Computer Engineering, Islamic Azad University Najafabad Branch, IRAN
dolatshahi@iaun.ac.ir

Abstract. This paper presents an optimized knowledge-based design approach for design of analog integrated circuits. The proposed design approach uses gm/ID technology characteristic in order to find the transistor dimensions (W, L) and drain currents. This method employs the gm/ID characteristic curve versus normalized drain current $I_D/(W/L)$ to calculate the design variables such as width (W) and length (L) of transistors in the circuit. As it is shown in the paper, the proposed method can be successfully used to minimize the power consumption of the analog integrated circuits.

Keywords: Analog, Low-power, Integrated circuits, CMOS.

1 Introduction

With the present trend toward the portable electronic devices, the design of analog integrated circuits is challenging due to the conflicting nature of the design objectives such as gain and bandwidth of an analog amplifier [1]. So, analog design automation tools are needed, to help the circuit designers. Many approaches have been reported in the literature [2-7]. However, most of them use mathematical equations to approximate the analog circuit’s behavior. Symbolic analysis, artificial neural network, fuzzy logic and geometric programming are examples of different approaches that have been used. However, proper modeling of both the devices (transistors) and the circuit are requirements which make the use of these tools more difficult in order to achieve the design objectives in a reasonable processing time.

However, in some applications, a combination of optimization algorithms and physical based models yields very good results for finding the optimal solution of analog integrated circuits design while a non-optimal solution has shortcomings for fully exploiting the capabilities of the analog CMOS technology.

A knowledge-based methodology which is successfully used to design of analog integrated circuits is gm/ID method which is first proposed in [2] and widely used in analog design automation [2-4]. This method uses the gm/ID curve as a technology characteristic and the knowledge of an expert analog designer to approximate the transistor dimensions (W, L) [2-4]. Since, this method uses transistors in all inversion regions such as weak, moderate and strong inversion region, the best trade-off be-
tween gain-bandwidth and power consumption can be achieved [3]. This paper organizes as follows: the gm/I₀ design methodology is briefly introduced in section 2. Section 3, presents the proposed design methodology while the simulation results are presented in section 4. Finally the conclusion is presented in section 5.

2 (gm/I₀)-Design approach

(gm/I₀) design methodology is a physics-based and optimal approach for designing analog integrated circuits which is based on a unique characteristic curve for a given technology. This curve is considered as the design tool and describes the relationship between the value of (gm/I₀) and the normalized current I_n = I_D/(W/L), for each transistor in the given technology. Since, gm/I₀ approach considers a size-independent, physical characteristic of the transistor which is the relationship between the ratio of transconductance (gm) over DC drain current versus normalized drain current I_n = I_D/(W/L) as a fundamental design parameter, this method gives a clear vision over the transistor operation region (weak, moderate, strong inversion) to the designer and provides a useful way for estimation of transistor dimensions. This method could also be very helpful especially in the low-power analog integrated circuit design, because this approach enables designer to choose the moderate inversion region to obtain a reasonable speed-power trade-off which is a key to success and the most challenging task in the low-power analog integrated circuit design [2]. Figure 1, shows the gm/I₀ curve versus normalized current I_n, this curve is divided into three regions: weak, moderate and strong inversion regions. The main characteristic of each region is summarized in table 1.

![Image of the diagram showing gm/I₀ curve versus normalized current I_n = I_D/(W/L)](image-url)

**Fig. 1.** (gm/I₀) curve versus normalized current I_n=I_D/(W/L)
Table 1. Main characteristic of each inversion region

<table>
<thead>
<tr>
<th>Inversion region</th>
<th>Characteristic of region</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weak Inversion</td>
<td>Low-power, High-gain</td>
</tr>
<tr>
<td>Moderate Inversion</td>
<td>Moderate gain and bandwidth</td>
</tr>
<tr>
<td>Strong Inversion</td>
<td>High-speed, High-power consumption</td>
</tr>
</tbody>
</table>

So, this \((\text{gm/ID})\) characteristic curve enables the designer to calculate the unknown transistor aspect ratio \((W/L)\) in the design procedure. While the values of \((\text{gm/ID})\) and \(I_D\) is chosen to fit the operation region of each transistor with a predefined role of each transistor according to table 1, the designer can determine the transistor dimensions \((W/L)\) by means of this universal characteristic.

3 Proposed design methodology

In this paper, a “folded-cascode” OPAMP is considered to design due to its high gain and bandwidth performances while it requires easier frequency compensation in comparison with two-stage OPAMPs. Figure 2, shows a Folded-Cascode OPAMP structure with transistors M1 and M2 as the input differential stage and transistors M4-M11 as Folded-Cascode stage.

![Folded-Cascode OPAMP structure](image)

Fig. 2. Folded-Cascode OPAMP structure
The performance measures for the OPAMP circuit are as follows:

- **Power dissipation (Pdiss):**

\[
P_{\text{diss}} = V_{\text{DD}} (I_3 + I_4 + I_5)
\]  

(1)

- **Open loop gain**

\[
A_o = \frac{g_{m1}}{g_{m8} r_{o8} + g_{o6} r_{o4}}
\]  

(2)

- **Unity gain frequency**

\[
w_c \approx \frac{g_{m1}}{C_L}
\]

Where, \(C_L\) is the total load capacitance at the output node.

- **Slew-Rate**

\[
\text{SR} = 2I_{D1}/C_L
\]  

(4)

- **Phase margin:**

A simple expression for the phase margin can be obtained as:

\[
PM = \frac{\pi}{2} - \arctan \left( \frac{w_c}{p_2} \right)
\]  

(5)

Where, \(p_2\) is the non-dominant pole at drain of \(M_{10}\) and is given by:

\[
p_2 = \frac{g_{m8}}{c_{d10} + c_{gd10} + c_{dd1} + c_{ks8} + c_{bs8}}
\]  

(6)

Fig. 3, illustrates the design methodology for transistor \(M1\) in the Folded-Cascode OPAMP circuit. As it is obvious in the above equations, \(M1\) has an effective role in the performance measures such as bandwidth, gain and slew-rate.

To calculate the dimensions of transistors \(M1\), according to the required power consumption and slew-rate of the circuit, the transistor DC current \(I_0\) is determined. Next, according to the desired value of bandwidth, \(g_{m1}\) is determined. So, the value of \(g_{o}/I_0\) for \(M1\) will be calculated and the corresponding \(I_0/(W/L)\) is determined using the \(gm/I_0\) characteristic curve in fig. 1. However, according to the resulted value of
\( I_D/(W/L) \) and the value of DC current of the transistor M1, the transistor dimensions can be achieved. Finally, for other transistors a similar algorithm can be used to calculate the transistor dimensions.

**Fig.3.** design algorithm of transistor M1 for Folded-Cascode OPAMP

### 4 Simulation results

In order to verify the performance of the proposed design algorithm, the folded cascode OPAMP is successfully designed and simulated using 0.18\( \mu \)m CMOS technology parameters in HSPICE. Table 2 summarizes the resulted \( g_m/I_D \) value for each transistor while table 3 summarizes the OPAMP performance measures obtained from circuit simulations in HSPICE.

**Table 2.** \( g_m/I_D \) value resulted for each transistor

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>( g_m/I_D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,2</td>
<td>15</td>
</tr>
<tr>
<td>M3</td>
<td>3</td>
</tr>
<tr>
<td>M4,5</td>
<td>5</td>
</tr>
<tr>
<td>M6,7</td>
<td>17</td>
</tr>
<tr>
<td>M8,9</td>
<td>23</td>
</tr>
<tr>
<td>M10,11</td>
<td>5.5</td>
</tr>
</tbody>
</table>
Table 3. Circuit performance obtained from HSPICE

<table>
<thead>
<tr>
<th>Performance measure</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power dissipation</td>
<td>418 µW</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>70 dB</td>
</tr>
<tr>
<td>Phase margin</td>
<td>72 degrees</td>
</tr>
<tr>
<td>Unity gain bandwidth</td>
<td>160 MHz</td>
</tr>
<tr>
<td>Swing</td>
<td>0.55 V_{pp}</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18µm</td>
</tr>
</tbody>
</table>

Figure 4, shows the AC performance simulation result in HSPICE. It is obvious that the simulated OPAMP circuit has a DC gain of 70 dB with a unity gain frequency of 160 MHz. Figure 5, shows the transient response of the circuit. It is obvious that the OPAMP circuit has a 0.55V_{pp} output swing.

Fig. 4. AC performance simulation result in HSPICE
Fig. 5. Simulation result for the transient response of the OPAMP circuit

5 Conclusion

In this paper, using the proposed method, a Folded-Cascode operational amplifier is successfully designed and simulated using 0.18μm CMOS technology parameters in HSPICE circuit simulator. HSPICE circuit simulation results show a DC gain of 70dB and a unity-gain frequency (GBW) of 160MHz with a phase margin of 72 degrees in a 1.5V power supply and the total power consumption is only 418µW.

References